Spartan®-6 LX150T Development Kit
Hardware Co-Simulation Reference Design User Guide

Version 0.8
## Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Description</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8</td>
<td>Preliminary. Branched off from IVK EDK Reference Design User Guide.</td>
<td>Apr. 01, 2010</td>
</tr>
</tbody>
</table>
Table of Contents

Revision History ........................................................................................................................... - 1 -
Table of Contents ....................................................................................................................... - 2 -
Table of Figures ........................................................................................................................ - 3 -
Introduction .................................................................................................................................. 4 -
  Requirements .............................................................................................................................. 4 -
    Software .................................................................................................................................. 4 -
    Hardware ................................................................................................................................. 4 -
  Setup ........................................................................................................................................ 5 -
    Connecting the Xilinx Platform Cable USB-II JTAG programming cable ......................... 5 -
    Connecting the Ethernet Cable ............................................................................................ 6 -
    Connecting the 12V Power Supply ....................................................................................... 6 -
  Ethernet NIC Configuration ...................................................................................................... 7 -
What is Xilinx System Generator ? ............................................................................................. 12 -
What is Hardware Co-Simulation ? ........................................................................................... 13 -
What is the Avnet Spartan-6 LX150T Hardware Co-Simulation Compilation Target ? .......... 14 -
How do I install the Avnet Spartan-6 LX150T Hardware Co-Simulation Compilation Target ? - 15 -
Using Hardware Co-Simulation to Validate a 5x5 Video Filter Kernel ...................................... 16 -
  For more information … ..................................................................................................... 26 -
## Table of Figures

- Figure 1 – Setup - Connecting the Xilinx Platform Cable USB-II ................................................ - 5 -
- Figure 2 – Setup - Connecting the Ethernet Cable ................................................................. - 6 -
- Figure 3 – Setup – Connecting the 12V power supply .............................................................. - 6 -
- Figure 4 – Network Connections – Local Area Connection Properties ................................. - 7 -
- Figure 5 – Accessing the NIC manufacturer’s configuration GUI ........................................... - 8 -
- Figure 6 – Flow Control – Auto ............................................................................................. - 9 -
- Figure 7 – Flow Control – Generate & Respond ................................................................. - 9 -
- Figure 8 – Speed & Duplex – Auto .................................................................................. - 10 -
- Figure 9 – Jumbo Frames – Enabled .................................................................................. - 11 -
- Figure 10 – Xilinx System Generator – design example ...................................................... - 12 -
- Figure 11 – Hardware Co-Simulation .................................................................................. - 13 -
- Figure 12 – Hardware Co-Simulation Compilation Targets ............................................... - 14 -
- Figure 13 – Hardware Co-Simulation Installation – Contents of directory .......................... - 15 -
- Figure 14 – Hardware Co-Simulation Installation – Executing setup.m script ..................... - 15 -
- Figure 15 – 5x5 Video Filer Kernel – Opening the model .................................................. - 16 -
- Figure 16 – 5x5 Video Filer Kernel – Selecting the Avnet S6-LX150T target ...................... - 17 -
- Figure 17 – 5x5 Video Filer Kernel – Generating ............................................................... - 18 -
- Figure 18 – 5x5 Video Filer Kernel – Hardware Co-Simulation Library ............................... - 18 -
- Figure 19 – 5x5 Video Filer Kernel – Instantiating the Hardware Co-Simulation block .......... - 19 -
- Figure 20 – 5x5 Video Filer Kernel – Basic Configuration ............................................... - 20 -
- Figure 21 – 5x5 Video Filer Kernel – Ethernet Configuration ............................................ - 21 -
- Figure 22 – 5x5 Video Filer Kernel – JTAG Configuration ............................................... - 22 -
- Figure 23 – 5x5 Video Filer Kernel – Starting Co-Simulation ............................................. - 23 -
- Figure 24 – 5x5 Video Filer Kernel – Initialization Phase ................................................... - 24 -
- Figure 25 – 5x5 Video Filer Kernel – Co-Simulation Results ............................................. - 25 -
- Figure 26 – xlDoc – System Generator Help System .......................................................... - 26 -
- Figure 27 – PDF Documentation – System Generator Book List ......................................... - 27 -
Introduction

Xilinx System Generator provides hardware co-simulation, making it possible to incorporate a design running in an FPGA directly into a Simulink simulation. "Hardware Co-Simulation" compilation targets automatically create a bitstream and associate it to a block. When the design is simulated in Simulink, results for the compiled portion are calculated in hardware. This allows the compiled portion to be tested in actual hardware and can speed up simulation dramatically.

The Avnet hardware co-simulation compilation targets provide co-simulation support for Avnet boards using a raw Ethernet connection (called Point-to-point Ethernet in Xilinx System Generator). Point-to-point Ethernet co-simulation provides a straightforward high-performance co-simulation environment using a direct, point-to-point Ethernet connection between a PC and FPGA platform.

Requirements

The software and hardware requirements for this kit are described in the following sections.

Software

The software required to use and run the demonstrations is:

- WindowsXP 32-bit
- Xilinx ISE Design Suite 11.4 : DSP Edition or System Edition
- MathWorks software Release 2009b

Hardware

The additional hardware required to run these demonstrations is:

- Computer with a minimum of 950 MB to complete a design
- Xilinx® Spartan®-6 LX150T PCI Express Development Kit
- 12V AC/DC adapter
- Xilinx Platform Cable USB II (or equivalent)
- Ethernet cable

---

1 All Xilinx Service Packs are available at www.xilinx.com/download
2 Refer to www.xilinx.com/ise/products/memory.htm
Setup

Perform the following steps to setup the hardware for running hardware co-simulation.

Connecting the Xilinx Platform Cable USB-II JTAG programming cable

Connect the USB-B end of the cable to the Xilinx Platform Cable USB-II. Connect the flat cable to the Spartan-6 LX150T development board’s J9 connector as shown in Figure 1.

![Figure 1 - Setup - Connecting the Xilinx Platform Cable USB-II](image-url)
Connecting the Ethernet Cable

Connect the Ethernet cable into the Spartan-6 LX150T carrier board’s J1 connector as shown in Figure 2. Connect the other end of the Ethernet cable to the PC.

![Figure 2 – Setup - Connecting the Ethernet Cable](image)

Connecting the 12V Power Supply

Plug in the 12V power adapter to the local AC power. Ensure that the power switch SW11 is in the off position. Plug the 12V power jack into the Spartan-6 LX150T carrier board’s J16 connector. Turn on the power by switching the SW11 to the "ON" position.

![Figure 3 – Setup – Connecting the 12V power supply](image)
Ethernet NIC Configuration

To achieve the maximum bandwidth during hardware co-simulation, your NIC (Network Interface Card) must be configured properly.

Not all NIC manufacturers display their configuration GUI the same way. For this reason, several examples will be shown on how to configure the NIC settings.

To configure the settings of your NIC, perform the following steps:

1) From the Start menu, select Control Panel, then select Network Connections

2) Right-click on your Local Area Connection, then select Properties.

![Figure 4 – Network Connections – Local Area Connection Properties](image-url)
3) Click on the **Configure** button to access the NIC manufacturer’s configuration GUI.

![Configure button on NIC properties](image)

**Figure 5 – Accessing the NIC manufacturer’s configuration GUI**
4) Xilinx recommends setting **Flow Control** to **Auto**
   
a. Under the **Advanced** tab, select **Flow Control** and select **Auto** as shown below

   ![Figure 6 – Flow Control – Auto](image)

b. If you don’t have any **Auto** choice available, as shown in the following examples, then select **Generate & Respond**

   ![Figure 7 – Flow Control – Generate & Respond](image)
5) Xilinx recommends setting **Speed & Duplex** to **Auto**

a. Under the **Advanced** tab, select **Speed & Duplex** and select **Auto** as shown in the first example. This setting could also be found in the **Link Speed** tab as shown in the second example.

![Figure 8 – Speed & Duplex – Auto](image-url)
6) For boards which support 1Gbps bandwidth, enabling the **Jumbo Frames** setting is strongly recommended to maximize the bandwidth usage.

![Jumbo Frames - Enabled](image)

**Figure 9 – Jumbo Frames – Enabled**
What is Xilinx System Generator?

“System Generator is a DSP design tool from Xilinx that enables the use of The Mathworks model-based design environment Simulink for FPGA design. Previous experience with Xilinx FPGAs or RTL design methodologies is not required when using System Generator. Designs are captured in the DSP friendly Simulink modeling environment using a Xilinx specific blockset. All of the downstream FPGA implementation steps including synthesis and place and route are automatically performed to generate an FPGA programming file.”

For more information on Xilinx System Generator, consult the dedicated page on the Xilinx web site:

http://www.xilinx.com/ise/optional_prod/system_generator.htm

---

What is Hardware Co-Simulation?

"System Generator provides accelerated simulation through hardware co-simulation. System Generator will automatically create a hardware simulation token for a design captured in the Xilinx DSP blockset that will run on one of over 20 supported hardware platforms. This hardware will co-simulate with the rest of the Simulink system to provide up to a 1000x simulation performance increase."\(^4\)

\(^4\) Excerpt from “System Generator for DSP – Getting Started Guide”, Release 10.1.3 September, 2008
What is the Avnet Spartan-6 LX150T Hardware Co-Simulation Compilation Target?

The Avnet Spartan-6 LX150T hardware co-simulation compilation target provides co-simulation support for the Avnet Spartan-6 LX150T Base Kit using either of the following connections:
- JTAG connection
- raw Ethernet connection (called Point-to-point Ethernet in Xilinx System Generator)

Point-to-point Ethernet co-simulation provides a straightforward high-performance co-simulation environment using a direct, point-to-point Ethernet connection between a PC and FPGA platform.

Once installed, this compilation target will appear in the Xilinx System Generator token as shown below …

![Figure 12 – Hardware Co-Simulation Compilation Targets](image)
How do I install the Avnet Spartan-6 LX150T Hardware Co-Simulation Compilation Target?

The Avnet Spartan-6 LX150T Hardware Co-Simulation Compilation Target does not ship with the Xilinx software and must therefore be installed.

In order to install this plug-in, open Matlab and change directory to the following location:

```
{Installation directory}\HWCOSIM_Installation\n```

You should see something like the following:

![Figure 13 – Hardware Co-Simulation Installation – Contents of directory](image)

Type the “setup” command which will call the “setup.m” script. This will install the hardware co-simulation compilation target for each of the supported Avnet boards.

![Figure 14 – Hardware Co-Simulation Installation – Executing setup.m script](image)
Using Hardware Co-Simulation to Validate a 5x5 Video Filter Kernel

This section assumes that the hardware has been correctly setup:

- JTAG connected to the S6-LX150T carrier's J9 connector
- Ethernet connected to the S6-LX150T carrier's J1 connector

Refer to the Getting Started Guide [Ref Error! Reference source not found.] for information on setting up the IVK hardware. If the demo fails to run, see the Error! Reference source not found. Appendix.

Now that the hardware co-simulation target is installed, we will demonstrate how to use it to validate a 5x5 video filter kernel.

Open Matlab and change directory to the following directory:

\{XILINX\}\DSP_Tools\int\sysgen\examples\shared_memory\hardware_cosim\conv5x5_video

where \{XILINX\} is the location where Xilinx was installed (ie. C:\\Xilinx\11.1)

Open the conv5x5_video_ex.mdl model.

![Figure 15 – 5x5 Video Filter Kernel – Opening the model](image)
Double-click on the System Generator block and select one of the Avnet Hardware Co-Simulation compilation targets as shown below …

![System Generator: conv5x5_video_ex window](image)

**Figure 16 – 5x5 Video Filer Kernel – Selecting the Avnet S6-LX150T target**

**Note**: The Point-to-Point Ethernet hardware co-simulation target will only work with version 12.1 of the Xilinx tools. If you don’t have this version yet, select the JTAG hardware co-simulation target instead.
Click on Generate to build the design for hardware co-simulation … this will take a while, so be patient …

![Compilation status](image1)

**Figure 17 – 5x5 Video Filer Kernel – Generating**

When the build process completes, a hardware co-simulation block will appear in a new `conv5x5_video_ex_hwcosim_lib.mdl` library. Do not close the hwcosim library. Click on the OK button in the Compilation status dialog box.

![Compilation status](image2)

**Figure 18 – 5x5 Video Filer Kernel – Hardware Co-Simulation Library**
Open the conv5x5_video_testbench.mdl model and drag the “conv5x5_video_ex hwcosim” block into the testbench model as shown below …

Figure 19 – 5x5 Video Filer Kernel – Instantiating the Hardware Co-Simulation block
Double-click on the “conv5x5_video_ex hwcosim” block, select the **Basic** tab, and set the Clock source to **“Free running”**.

*Figure 20 – 5x5 Video Filer Kernel – Basic Configuration*
If you are using JTAG hardware co-simulation, skip this step and proceed to the next page.

If you are using the Point-to-Point Ethernet hardware co-simulation, you need to configure the Ethernet connection.

Select the Ethernet tab, and select your PC's Ethernet connection from the Host interface drop down list.

![Figure 21 – 5x5 Video Filer Kernel – Ethernet Configuration](image)
Select the **Configuration** tab, and select your Xilinx JTAG cable from the available choices.

![Configuration tab screenshot](image)

Figure 22 – 5x5 Video Filer Kernel – JTAG Configuration

Click OK to close the "conv5x5_video_ex_hwcosim" parameters dialog box.
Press the play button to start the hardware co-simulation

![5x5 Video Filer Kernel – Starting Co-Simulation](image)

**Figure 23 – 5x5 Video Filer Kernel – Starting Co-Simulation**
The simulink model will first download the bitstream via JTAG, then it will establish a link with the FPGA design via Ethernet or JTAG.
The model will run the FPGA in the loop co-simulation until the user stops the simulation.

Figure 25 – 5x5 Video Filer Kernel – Co-Simulation Results
For more information ...  

For more information on Xilinx System Generator hardware co-simulation, consult the System Generator documentation. This documentation can be accessed in two ways:

From MATLAB, type the "xlDoc" command to launch the System Generator Help System.

**Using Hardware Co-Simulation**

**Introduction**

System Generator provides hardware co-simulation, making it possible to incorporate a design running in an FPGA directly into a Simulink simulation. "Hardware Co-Simulation" compilation targets automatically create a bitstream and associate it to a block. When the design is simulated in Simulink, results for the compiled portion are calculated in hardware. This allows the compiled portion to be tested in a real hardware and can speed up simulation dramatically.

**M-Code Access to Hardware Co-Simulation**

It is possible to programmatically control the hardware created through the System Generator hardware co-simulation flow using MATLAB M-code (M-HwSim). The M-HwSim interfaces allow for MATLAB objects that correspond to the hardware to be created in pure M-code, independent of the Simulink framework. These objects can then be used to read and write data into Hardware. This capability is useful for providing a scripting interface to hardware co-simulation, allowing the hardware to be used in a scripted test bench or deployed as hardware acceleration in M-code.

For more information of this subject, refer to the topic "M-Code Access to Hardware Co-Simulation" in the section Programmatic Access.
From the Windows Start Menu,
select Programs => Xilinx ISE 11.1 Design Suite => DSP Tools => Documentation
click on the "Xilinx System Generator Manual" to access an index of all System Generator documents

Figure 27 – PDF Documentation – System Generator Book List